OIPE JC176 JAN 23 2003 PATENT & TRADEMARK OFFICE

2811

09/944665

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of
Toshiharu Furukawa et al.
Serial No.: ~~09/994,665~~ incorrect ser#
Filed: August 31, 2001
For: VERTICAL DUAL GATE FIELD EFFECT TRANSISTOR

Group Art Unit: 2811
Examiner: S. Loke

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Commissioner of Patents and Trademarks
Washington, D.C. 20231

AMENDMENT UNDER 37 C. F. R. §1.111

Sir:

In response to the Office Action mailed October 23, 2002, please amend the above-identified application as follows:

In the Specification:

Please substitute the following paragraphs for the corresponding paragraphs beginning at the indicated location in the specification as originally filed. A marked up copy of these paragraphs showing currently requested changes is attached as an Appendix to this response.

Page 9, line 16+:

Referring now to Figures 5A - 5C, the position of a mold for forming the vertical silicon pillar which will form the vertical conduction channel of the transistor is defined by application of a resist 510. The resist is then exposed using a hard phase shift mask or other lithographic process or other process techniques such as spacers to control width and developed to form a narrow (possibly of sub-lithographic width) linear pattern 520 across the non-STI region. Then, in accordance with the patterned